

Low Voltage Power Supply

Technical Description and User's Manual

1

© 2001 AREM PRO, Ltd.

Low Voltage Power Supply Technical description and User's Manual

1. Edition, October 2001

Published by AREM PRO, Ltd.

AREM PRO, Ltd., Nušlova 2275/15, 155 00 Prague 5, Czech Republic, tel/fax: +420 2 5162 1228

Contents

| 1. | INTRODUCTION | 5 |
|---------|--|----|
| 2. | BLOCK SCHEME DESCRIPTION | 6 |
| 3. | DETAILED SCHEME DESCRIPTION OF THE LVPS MODULE | 7 |
| 3.1. | SHEET 1 DESCRIPTION | |
| 3.2. | SHEET 2 DESCRIPTION | |
| 3.3. | SHEET 3 DESCRIPTION | |
| 3.4. | SHEET 4 DESCRIPTION | |
| 4. | LVPS APPLICATION | 9 |
| 4.1. | REGULATION SCHEME | 9 |
| 4 | 4.1.1. Internal analog regulator | 9 |
| 4 | 1.1.2. Software regulator | |
| 4 | 4.1.3. Error conditions | |
| 4.2. | LOAD CONNECTION | |
| 5. | SLOW CONTROL PROTOCOL | |
| 5.1. | PHYSICAL INTERCONNECTION | |
| 5.2. | . SW PROTOCOL | |
| 5. | 5.2.1. Command frame | |
| 5. | 5.2.2. Response frame | |
| 5. | 5.2.3. Object types and corresponding frames | |
| 5. | 5.2.4. Group reading | |
| 5. | 0.2.5. Error responses | |
| 5.3. | IMPLEMENTED VARIABLES | |
|). 5 | 5.2.1. BINARY | |
| 5 | 5.3.2. Real | |
| 5 | .J.J. Keu | |
| 6. | TECHNICAL SPECIFICATION | |
| 6.1. | LVPS MODULE | |
| 6.2. | . SMALL LVPS RACK | |
| 6.3. | STANDARD LVPS RACK | 23 |
| 7. | RACK REAR PANEL CLAMPS DESCRIPTION | |
| 8. | SCHEMES AND PCB LAYOUT | |
| 8.1. | LVPS SCHEME, SHEET1 | |
| 8.2. | LVPS SCHEME, SHEET2 | |
| 8.3. | LVPS SCHEME, SHEET3 | |
| 8.4. | LVPS SCHEME, SHEET4 | |
| 8.5. | . LVPS PCB LAYOUT, COMPONENT SIDE | |
| 8.6. | . LVPS PCB LAYOUT, SOLDER SIDE | |

1. Introduction

The Low Voltage Power Supply (LVPS) is a modular power supply system for detectors and adjacent electronic circuits for Alice experiments. The basic component of the system is a LVPS module. The LVPS module is designated for 6HE racks, that can according to their size contain 4 (small racks) or 8 (19'' standard racks) LVPS modules. A backplane of the rack provides the interconnection for the communication among the individual LVPS modules and power outputs from the power supplies of the modules. The standard 19'' rack and the LVPS module are on the Fig. 1



Fig. 1 The rack and one LVPS module

Because of long cables for detector power provision (about tens of meters), the power supplies have to cover power consumption not only of detectors but also losses on the long cables. Each detector will be provided by an analog voltage stabilizer and output voltage of the power supplies have to be controlled to assure reasonable enough voltage for the detector stabilizer with respect to the immediate detector power consumption (in time interval of 10 ms) and corresponding losses on the cables. The voltage on the detector stabilizer is acquired through sense inputs evaluated by a microcomputer, which is responsible for the proper output voltage adjustment. The microcomputer also measures current on all power outputs to provide the current limitation according to user's requirements. To satisfy energy consumption during short current peaks (microseconds), it is necessary to install proper capacitors (about miliFarads) on the detector stabilizer voltage inputs.

Each LVPS module consists of two identical low voltage sections A and B, and each sections contains four independent power supplies. All power supplies have adjustable output voltage from 2.5 V to 7.5 V DC. The maximum output current of power supplies is 4A or 1A. The total power output per section has to be bellow 50W.

The individual power supplies in one LVPS module (both sections) are not galvanically isolated, but the mutual resistance between them is high (above 10 kiloOhms). Therefore, it is possible to combine power supplies as independent, but with some limitations mentioned later. However, the single LVPS modules in the rack are fully galvanically isolated.

2. Block scheme description

The block scheme of the LVPS module is shown on the Fig. 2. As it was previously mentioned, the LVPS module consists of two identical sections of power supplies A and B.

Both sections of the LVPS module have their 230V AC transformers to guarantee the galvanic separation from the electric network. Diode bridges with proper capacitors rectify the AC outputs of the transformers. The power supplies' regulators are based on the switching technology with the frequency of 300 kHz.



Fig. 2 The block scheme of the LVPS module

The whole LVPS unit is controlled by a microcomputer. The microcomputer is based on the Z80181 microprocessor with 128kB Flash EPROM, 128kB RAM and 2kB EEPROM to store the setting and the calibration of the individual power supplies. The microcomputer is equipped with RS232, RS485, JTAG interfaces and with galvanically separated input and output lines; the CAN interface is not supported by the contemporary software. Furthermore, the microcomputer guarantees the diagnostics of the module and indicates the current status on the front panel.

To control power supplies, microcomputer can adjust the power supply voltage outputs through D/A converters and can measure the sense voltage and output current through A/D converters. During the module operation, the microcomputer evaluates the sense voltage and output current of each power supply, compares them with required values and according to them decides about control action.

3. Detailed scheme description of the LVPS module

The scheme of the LVPS module consists of 4 sheets. These sheets and PCB layout are available at the end of the manual in chapter 8.

3.1. Sheet 1 description

The first sheet contains mainly the control microcomputer. The microcomputer is based on Z80181 (U1) microprocessor, equipped with Flash EPROM (U2) for control program, RAM (U3) for data and serial EEPROM (U5) for the system setting and calibration constants. To guarantee a proper start of the microcomputer after power on and the watch-dog function, the microcomputer is equipped with the MAX691 (U4) circuit. Majority of the microcomputer's glue logic is concentrated in the programmable logic array ispLSI1032 (U16); the latch HT273 (U6) serves for the power supplies' switching on/off.

The communication circuits are also placed on the sheet one. Firstly, the RS232 serial interface utilizes the MAX232A (U9) circuit. The MAX232 (U9) circuit produces also negative voltage for analogue circuits in the LVPS module. Furthermore, the RS485 interface for the intermodular communication in the rack is equipped with the MAX485 (U7, U8) circuits. The galvanically isolated JTAG interface comprizes the optocouplers (O1 - O3), the Schmitt inverter HCT14 (U11) and the MAX485 (U12 – U15) interface circuits. The CAN communication consists of the SAJ1000 (U17) controller, the optocouplers (O6, O7) and the driver 82C250 (U18).

The microcomputer also provides galvanically isolated binary inputs and outputs, which are intended for the safety functions. The optocouplers (O4, O5) and the transistors (T1, T2) assure these functions.

The indicators (LED1 – LED12) of the module's status are placed on the front panel of the module.

Lastly, the microcomputer measures the temperature of the module by the DS1621 (U10) digital thermometer.

3.2. Sheet 2 description

The second sheet of the LVPS scheme contains analog functions of the module. There are the D/A converters MAX534 (U19, U20) each with four analogue outputs there. These converters control output voltage of the power supplies (see Sheet 3 and 4 description).

The A/D converters MAX186 (U21, U23) are responsible for the sense voltage measurements. These voltage measurements are basis for the control function to provide the proper voltage for the detector's stabilizers and the adjacent electronics. The maximum voltage on the inputs of the A/D converters is \pm -4V. Thus, the power supplies can be interconnected in a manner that doesn't exceed this limit. Because of divider consisting of resistors 4k7 (R20, R22 etc.) versus the multiresistor 1k5 (MR7), the maximum voltage on the sense inputs has to be bellow \pm -16V. This condition establishes one limitation of the independent connection of the power supplies' outputs (see also chapter 4.2).

The A/D converter MAX186 (U22) provides the output current measurement. The A/D converter collaborates with the operational amplifiers MAX479 (U24 – U27). These amplifiers amplify the loss of voltage on the resistors for the current measurement (R72, R76, R80, etc.). Because of the input voltage limits \pm 4V of the operational amplifiers and dividers consist of the 10k (R52, R52A, etc.) and 10k (R51, R51A, etc.) resistors, the voltage on the current measurement resistors versus microcomputer ground have to be bellow \pm 8V. This is the second reason of limitation of the independent connections of the power supplies' outputs.

The stabilizer 79L05 (U39) provides -5V supply for the analog circuits. Its input voltage -10V is produced by the MAX232 (U9) circuit (see Sheet 1 description).

3.3. Sheet 3 description

The third sheet consists mostly of circuits providing galvanically isolated analogue signals to control the output voltage of the power supplies. Each circuit consists of the operational amplifier MAX4330 (U40 – U47) and the linear optocoupler HCNR4200 (O8 – O15). The linear optocouplers contains one LED and two photodiodes. One photodiode is utilized in the operational amplifier feedback, the other one as the output current source.

The remaining optocouplers PC847 (O16, O17) on the sheet provide galvanic isolation of the power supplies' switch on/off signals that come from the HT273 (U6) circuit (see Sheet 1 description).

3.4. Sheet 4 description

The fourth sheet of the LVPS scheme contains the power supplies. There are two sections of the power supplies named A and B. Each section consists of 4 switching power supplies. Their names are A1A, D1A, D2A a D3A for the section A and A1B, D1B, D2B, D3B for the section B respectively. All of the power supplies provide voltage according to the D/A converters (see Sheet 2 description) control signals with the galvanic isolation (see Sheet 3 description) in the range of 2.5V - 7.5V. The output current for the A1A, D3A, A1B and D3B power supplies is maximal up to 4A, for the D1A, D2A, D1B, D2B is maximal up to 1A. The total power output in one section cannot exceed 50W. Each power supply can be switched on/off by the control microcomputer (see U6 in Sheet 1 description and O16, O17 in Sheet 3 description).

Each power supply consists of diode bridge rectifier, capacitors, integrated circuits LM2678-A (up to 4A current) or LM2675-A (up to 1A current), proper inductors and diodes. To reduce output voltage noise, there is a LC filter on the output of each power supply. As previously mentioned, the power supplies are independent but not galvanically isolated. It is possible to interconnect power supplies outputs to achieve positive or negative output voltage but this voltage cannot exceed limits mentioned in the paragraph Sheet 2 description (see also chapter 4.2).

Moreover, there are other three power supplies on this sheet. The first one (based on U32 integrated circuit) provides the power supply +5V for the microcomputer and digital logic, the second one (U33) is galvanically isolated power supply +5V for the JTAG interface and the third one (U34) is galvanically isolated power supply +5V for the CAN interface.

4. LVPS application

4.1. Regulation scheme

As mentioned above, there are two regulators that are responsible of LVPS output voltage.

- 1. internal analog HW regulator
- 2. external SW regulator



Fig. 3 Regulation scheme

In following section some examples of transient waveforms are given. These are measured on sections D2A, D2B, D3A and D3B. Waveforms for other LVPS sections are similar.

4.1.1. Internal analog regulator

Internal analog regulator controls the Switched Power Supply (SPS). Required voltage is defined by DAC and insulating amplifier. (IA). The time constant of its response is defined by "internal resistance" of SPS and value of SPS output capacitor. (Fig. 4, Fig. 5).

| 1 5000 | .00.00 | s 1.00g/ | ∱1 RUN |
|--------|---------------------------------------|---|---------------|
| | | | |
| | ···· | | |
| | <u>+</u> | A. S. | |
| | | | |
| | ±/ | | |
| | | | |
| | | | |
| | · · · · · · · · · · · · · · · · · · · | | |
| | ····· <u>†</u> ······ | | |
| | | | |
| | ····· | | |
| | | | |

Fig. 4 Internal analog regulator response (U_{out}) to the required value change from 1.2V to 3V in section D2B. R_L=4.7Ohm, R_W=2*1.5Ohm, C_L=0. Software regulator is off.



Fig. 5 Internal analog regulator response (U_{out}) to the required value change from 3V to 0V in section D2B. R_L=4.70hm, R_W=2*1.50hm, C_L=0. Software regulator is off.

When the load resistor R_L is connected with parallel capacitor C_L , the response is slower. (Fig. 6, Fig. 7)



Fig. 6 Internal analog regulator response (U_{out}) to the required value change from 0V to 1V then to 3V in section D2A. R_L=4.7Ohm, R_W=2*1.5Ohm, C_L=2.2mF. Software regulator is off.



Fig. 7 Internal analog regulator response (U_{out}) to the required value change from 5V to 0V. in section D2A. R_L =4.70hm, R_W =2*1.50hm, C_L =2.2mF. Software regulator is off.

The internal regulator doesn't produce oscillations of output voltage in any case of expected load characteristic.

4.1.2. Software regulator

Software regulator reads S+ and S- voltage and controls the DAC output to set the difference between S+ and S- to required value. This way it compensates loss on R_W resistance of connecting wires and slow load changes. During regulation it checks special error conditions.



Fig. 8 SW regulator response (U_L) to the required value change from 2V to 4V in section D3B. R_L =2.2Ohm, R_W =2*0.68Ohm, C_L =0mF. Software regulator is on.



Fig. 9 SW regulator response (U_L) to the required value change from 4V to 2V in section D3B. R_L =2.20hm, RW=2*0.680hm, C_L=0mF. Software regulator is on.



Fig. 10 SW regulator response (U_L) to the load change from R_L =2.20hm to R_L =1.10hm and back in section D3B. R_W =2*0.680hm, C_L =0mF. Software regulator is on.

The time constant of regulator is approximately 5ms. This time constant may change with SW version but it will not exceed 10ms. Following pictures show SW regulator responses in various situations.



Fig. 11 SW regulator response (U_L) to the required value change from 1.2V to 4V in section D3A. R_L =2.2Ohm, R_W =2*0.68Ohm, C_L =2.2mF. Software regulator is on.



Fig. 12 SW regulator response (UL) to the required value change from 4V to 1.2V in section D3A. R_L =2.2Ohm, R_W =2*0.68Ohm, C_L =2.2mF. Software regulator is on.



Fig. 13 SW regulator response (U_L) to the load change from R_L =2.20hm to R_L =1.10hm and back in section D3A. R_W =2*0.680hm, C_L =2.2mF. Software regulator is on.

The SW regulator time constant of 5ms is slow enough to make regulator stable and quick enough for reaction to the load changes. Expected very fast reversible load changes producing current pulses can not be compensated by any kind of regulator because of electrical characteristic of leading wires. Current pulses can be satisfactory compensated by capacitor C_L . The DAC allows to set the output voltage in cca 30mV steps.

4.1.3. Error conditions

Software regulator checks the load connection and recognises following error conditions.

- 1. Overcurrent SPS current exceeds user defined limit
- 2. No load Sense voltage is 0, current is 0.
- 3. Short circuit R_L is less then 0.50hm. This condition can exist without producing overcurrent.

4.2. Load connection

There are several rules for load connection.

- 1. To obtain the set voltage on the load resistor, it is necessary to connect sense wires to the load, not to the output clamps P+, P- of the LVPS module. This simplified connection is possible only for very short distances to the load, where the loss on leading wires is negligible. Do not worry about oscillations. The time constant of SW regulator is long and internal analog regulator is not affected by S+ and S- at all.
- 2. All loads of one LVPS module connect to one node and this node connects to GND clamp of LVPS module. This connection is not strictly necessary, but is recommended. It minimises the voltage offset of current measuring resistor and then produces minimal error of current measuring differential amplifier. When the precision of current measurement is not important, connection is not necessary. See Fig. 14 and Fig. 15
- 3. Serial connection of sources is possible. Limitation is on maximum voltage between S+ or S- to GND that is 16 V. See Fig. 16.
- 4. GND clamp is connected to the microprocessor GND and to the RS232 GND. When you need load or microprocessor insulated from slow control microcomputer, use external serial line insulator.
- 5. LVPS modules in rack are insulated from each other. Due to the serial interconnection via backplane the maximum voltage between GND nodes of LVPS modules can be 50V.



Fig. 14 Load and GND connection, all voltages positive to GND



Fig. 15 Load and GND connection, some voltages positive, some negative



Fig. 16 Serial connection of two power supplies of LVPS module

5. Slow control protocol

In this section the slow control protocol for data acquisition and control LVPS modules is described.

5.1. Physical interconnection

Protocol is implemented on serial line RS232 (front panel of LVPS) with following setting.

Asynchronous mode

- 19200Bd
- 8 bit
- No parity
- 1 stop bit
- Data flow control RTS/CTS
- Connector on LVPS D9 Male

Each LVPS module in the rack has its own address defined by its position. When module receives frame from serial line, it checks its address. When the address equals to its address, module responds directly. When the address is not equal, module retranslates the frame to the backplane serial bus. (144kbps), gets the answer of the addressed module from backplane serial bus and retranslates it to the serial line RS232.

5.2. SW Protocol

The protocol is text oriented. All information is exchanged in frames containing "visible" ASCII characters and CR LF characters. LVPS modules are waiting for incoming frames and then responds. LVPS does not initiate communication

5.2.1. Command frame

Command frame is transmitted from supervisory system to LVPS. It consists of following parts:

| Introductory | Module | Command | Object | Object | Space | Data | End |
|--------------|---------|---------|--------|---------|-------|------|-----------|
| character | address | type | type | address | | | character |
| IC | MA | СТ | OT | OA | Space | D | CR |

Introductory character IC is ASCII '\$'.

Module address MA is one character in range '0' to '7' .(LVPS module address is defined by position in the rack by 3-bit code read from backplane.)

Command type CT – one character:

- ! set object value
- ? read object value
- N read object name

Object type OT – one character:

- B binary object
- I integer object
- R real object

Object address OA - two character decimal number. The range of address is given by number of objects of required type.

Space – ASCII space character (20 in hexadecimal code).

Data D – only in the case of "set value" commands. Format depends on the OT.

End character - ASCII character CR (0D in hexadecimal code).

5.2.2. Response frame

Response frame is transmitted from LVPS to supervisory system. It consists of following parts:

| Introductory character | Module address | Command | Response Data | End character |
|------------------------|----------------|---------|------------------|---------------|
| IC | MA | С | D | CR |

Introductory character IC is ASCII '\$' in positive case, ASCII '#' when error occurred (Negative response).

Module address MA is one character in range '0' to '7' .(LVPS module address is defined by position in the rack by 3-bit code read from backplane.)

Command C – the part of command frame containing CT,OT,OA,Space and D

Response data D – Object data in the case of read command or Error code in the case of error in the command field (Negative response). Negative responses will be discussed in separate chapter.

End character - ASCII character CR (0D in hexadecimal code).

5.2.3. Object types and corresponding frames

Binary variables

Binary variables are organised into 16-bit words. This word represents one addressable object. Every bit of word is R/W or Read only mode. The mode is defined by firmware and cannot be changed.

Value setting

Data field of command frame is string containing characters '0','1','x' and Space. Space characters are ignored. Other characters are organised in MSB – LSB order. That means, that the last character corresponds to the least significant bit of the word. Characters have following meaning.

| `0` `1` `x` | Set the bit to 0 Set the bit to 1 Leave the bit unchanged | | |
|-------------------|---|--|--|
| Example: | Command: Response: | \$3!B00 10xx0101 <cr> \$3!B00 10xx0101<cr></cr></cr> | |
| Example: | Command: Error resp.: | \$3!B16 1 <cr> #3!B16 1 IE<cr></cr></cr> | |
| Example: | Command: Error resp.: | \$3!B16 abc <cr> #3!B16 abc VE<cr></cr></cr> | |

Value reading

Data field of the response frame is 17 character string containing characters '0','1' and Space. The space character is used to separate two 8 character halves for better readability. 16 '0' or '1' characters are organised in MSB – LSB order.

| Example: | Command: Response: | \$3?B01 <cr> \$3?B01 00000101 10010111<cr></cr></cr> |
|----------|---------------------------|--|
| Example: | Command: Error resp.:. | \$3?B16 <cr> #3?B16 IE<cr></cr></cr> |
| Example: | Command: Error resp.: | \$3?X16 <cr> #3?X16 GE<cr></cr></cr> |

5.2.3.1. Integer variables

Integer variables are stored in 16-bit words. Every variable can be internally assigned as a R/W or Read only. LVPS firmware uses this values as a fixed point numbers. When set to read they appear as a real numbers. The decimal point position is fixed and is shown in the variable list later.

Value setting

The command frame data field contains decimal number in fixed point format.

| Example: | Command: | \$3!I08 | 13.8 <cr></cr> |
|----------|-----------|---------|----------------|
| | Response: | \$3!108 | 13.8 <cr></cr> |

Value reading

The response frame data field contains decimal number in fixed point format. Data always contains 5 numbers. Leading zeroes are always transmitted.

| Example: | Command: | \$3?I10 <cr></cr> |
|----------|-----------|---------------------------|
| | Response: | \$3?I10 +000.10 <cr></cr> |

5.2.3.2. Real variables

Real variables are internally represented in 32 bit format according to the IEEE 745. Every variable can be internally assigned as a R/W or Read only.

Value setting

The command frame data field contains decimal number in floating point format common in all programming languages. LVPS protocol requires at least one number before decimal point.

Example of valid strings:

```
1
1.28
-3.25E-3
```

Example: Command: \$3!R00 3.3<CR> Response: \$3!R00 3.3<CR>

Value reading

The response frame data field contains decimal number in 12 character floating point format <s><m.mmmm>E<s><ee>

| Example: | Command: | \$3?R01 <cr></cr> |
|----------|-----------|--------------------------------|
| | Response: | \$3?R01 +4.50000E+00 <cr></cr> |

5.2.4. Group reading

There are implemented two special command frames, for accessing the most commonly read values.

Reading values from section A

Command: \$3?a<CR>

The response data contains 12 numbers in fixed point format. Their meaning is following:

- 1. Load voltage A1A
- 2. Load current A1A
- 3. Output voltage A1A
- 4. Load voltage D1A
- 5. Load current D1A
- Output voltage D1A 6.
- 7. Load voltage D2A
- 8. Load current D2A
- 9. Output voltage D2A
- 10. Load voltage D3A
- 11. Load current D3A
- Output voltage D3A 12.

\$3?a<CR> Example: Command: \$3?a +3.50 +1.25 +5.20 +3.20 +0.65 +4.20 +3.20 +0.65 +4.20 Response:

+3.50 +1.25 +5.20 <CR>

Reading values from section B

Command: \$3?b<CR>

The response data contains 12 numbers in fixed point format. Their meaning is following:

- 1. Load voltage A1B
- 2. Load current A1B
- 3. Output voltage A1B
- 4. Load voltage D1B
- Load current D1B 5.
- 6. Output voltage D1B
- Load voltage D2B 7.
- 8. Load current D2B
- 9. Output voltage D2B
- 10. Load voltage D3B
- Load current D3B 11.
- 12. Output voltage D3B

| Example: | Command: | \$3?b <cr></cr> |
|--------------|-----------|--|
| | Response: | 3?a + 3.50 + 1.25 + 5.20 + 3.20 + 0.65 + 4.20 + 3.20 + 0.65 + 4.20 |
| +3.50 + 1.25 | | |

5.2.5. Error responses

You receive negative response in following situations:

| Situation | Response data |
|--|---------------|
| The slave module doesn't respond at all (module not connected via RS232) | Empty |
| The command type is not valid | Empty |
| The object type is not valid (group error) | "GE" |
| The object address is not valid or does not exist (index error) | "IE" |
| The data are not valid (value error) | "VE" |
| Attempt to write to the read only object (write error) | "WE" |

5.3. Implemented variables

5.3.1. Binary

| Addr | Name | $R/W \mod (w = R/W)$ | Description |
|------|------------------|----------------------|-------------------|
| 00 | A1A binary flags | wwwwwww rrrrrww | channel A1A flags |
| 01 | D1A binary flags | wwwwwwww rrrrrww | channel D1A flags |
| 02 | D2A binary flags | wwwwwwww rrrrrww | channel D2A flags |
| 03 | D3A binary flags | wwwwwwww rrrrrww | channel D3A flags |
| 04 | A1B binary flags | wwwwwww rrrrrww | channel A1B flags |
| 05 | D1B binary flags | wwwwwwww rrrrrww | channel D1B flags |
| 06 | D2B binary flags | wwwwwwww rrrrrww | channel D2B flags |
| 07 | D3B binary flags | wwwwwwww rrrrrww | channel D3B flags |
| 08 | Section A flags | wwwwwww wwwwwww | section A flags |
| 09 | Section B flags | wwwwwww wwwwwwww | section B flags |

Bits in words 00 to 07:

- Bit D0 Channel enable
- Bit D1 SW regulator enable
- Bit D8 Overcurrent detected
- Bit D9 Load disconnected
- Bit D10 Short circuit detected ($R_L < 0.5$ Ohm)
- Bit D15 Temperature limit reached

Bits in words 08 to 09:

- Bit D0 Section enable
- Bit D8 Overcurrent in any channel of section
- Bit D9 Load disconnected in any channel of section
- Bit D10 Short circuit detected in any channel of section
- Bit D15 Temperature limit reached..

The output voltage of channel is set if all following conditions are fulfilled:

- Section is enabled
- Required voltage is set
- Channel is enabled
- No error bit in section is set

We recommend the following sequence for setting up:

- 1. Set required voltage of all channels you want to use.
- 2. Select the SW regulator function
- 3. Enable channels you want to use.

4. Enable section.

When error is detected the recover procedure should be as follows.

- 1. Set error flags to 0
- 2. Enable channels
- 3. Enable section

5.3.2. Integer

| Addr | Name | Dec. point position | r/w | Description |
|------|--------------------|---------------------|-----|---------------------|
| 00 | A1A Status word : | xxxxx. | r | |
| 01 | D1A Status word : | xxxxx. | r | |
| 02 | D2A Status word : | xxxxx. | r | |
| 03 | D3A Status word : | xxxxx. | r | |
| 04 | A1B Status word : | xxxxx. | r | |
| 05 | D1B Status word : | xxxxx. | r | |
| 06 | D2B Status word : | xxxxx. | r | |
| 07 | D3B Status word : | xxxxx. | r | |
| 08 | Reg window [mV]: | xxxxx. | r/w | Regulator dead band |
| 09 | Module address = | xxxxx. | r | |
| 10 | Software version = | xxx.xx | r | |
| 11 | Serial number= | xx.xxx | r | |

Channel status word:

- 0 Off
- 1 On
- 2 Error status

5.3.3. Real

| Addr | Name | r/w | Description |
|------|----------------|-----|-----------------------------------|
| 00 | A1A V required | r/w | Required voltage |
| 01 | D1A V required | r/w | |
| 02 | D2A V required | r/w | |
| 03 | D3A V required | r/w | |
| 04 | A1B V required | r/w | |
| 05 | D1B V required | r/w | |
| 06 | D2B V required | r/w | |
| 07 | D3B V required | r/w | |
| 08 | A1A V ramp | r | For future use |
| 09 | D1A V ramp | r | |
| 10 | D2A V ramp | r | |
| 11 | D3A V ramp | r | |
| 12 | A1B V ramp | r | |
| 13 | D1B V ramp | r | |
| 14 | D2B V ramp | r | |
| 15 | D3B V ramp | r | |
| 16 | A1A Output V | r | Voltage on the channel output |
| 17 | D1A Output V | r | |
| 18 | D2A Output V | r | |
| 19 | D3A Output V | r | |
| 20 | A1B Output V | r | |
| 21 | D1B Output V | r | |
| 22 | D2B Output V | r | |
| 23 | D3B Output V | r | |
| 24 | A1A V on load | r | Voltage difference on sense nodes |
| 25 | D1A V on load | r | |
| 26 | D2A V on load | r | |

| Addr | Name | r/w | Description |
|------|---------------------|-----|-----------------------------------|
| 27 | D3A V on load | r | |
| 28 | A1B V on load | r | |
| 29 | D1B V on load | r | |
| 30 | D2B V on load | r | |
| 31 | D3B V on load | r | |
| 32 | A1A Load current | r | Current in channel |
| 33 | D1A Load current | r | |
| 34 | D2A Load current | r | |
| 35 | D3A Load current | r | |
| 36 | A1B Load current | r | |
| 37 | D1B Load current | r | |
| 38 | D2B Load current | r | |
| 39 | D3B Load current | r | |
| 40 | A1A Load resistance | r | Calculated load resistance |
| 41 | D1A Load resistance | r | |
| 42 | D2A Load resistance | r | |
| 43 | D3A Load resistance | r | |
| 44 | A1B Load resistance | r | |
| 45 | D1B Load resistance | r | |
| 46 | D2B Load resistance | r | |
| 47 | D3B Load resistance | r | |
| 48 | A1A Lead resistance | r | calculated resistance of wires |
| 49 | D1A Lead resistance | r | |
| 50 | D2A Lead resistance | r | |
| 51 | D3A Lead resistance | r | |
| 52 | A1B Lead resistance | r | |
| 53 | D1B Lead resistance | r | |
| 54 | D2B Lead resistance | r | |
| 55 | D3B Lead resistance | r | |
| 56 | A1A Current limit | r/w | Required current limit in channel |
| 57 | D1A Current limit | r/w | |
| 58 | D2A Current limit | r/w | |
| 59 | D3A Current limit | r/w | |
| 60 | A1B Current limit | r/w | |
| 61 | D1B Current limit | r/w | |
| 62 | D2B Current limit | r/w | |
| 63 | D3B Current limit | r/w | |
| 64 | Module temperature | r | |
| 65 | Temperature limit | r/w | Module temperature limit |

6. Technical Specification

6.1. LVPS module

Two identical low voltage sections A and B in one LVPS module

| Input voltage: | 230V AC |
|-----------------|--|
| Output voltage: | Section A 2.5-7.5V, current up to 4A 2.5-7.5V, current up to 1A 2.5-7.5V, current up to 1A 2.5-7.5V, current up to 4A total output power up to 50 W |
| | Section B 2.5-7.5V, current up to 4A 2.5-7.5V, current up to 1A 2.5-7.5V, current up to 1A 2.5-7.5V, current up to 4A total output power up to 50 W |

Output voltage noise: < 5 mV RMS

| Communication: | RS232 (slow control), JTAG (control and testing), RS485 (galvanically isolated communication among the LVPS units in the rack), CAN (optional, not supported by the software now) |
|----------------|---|
| Dimension: | 261mm * 295mm * 50.8mm |
| Weight: | 2.95 kg |

6.2. Small LVPS rack

Designated for up to 4 LVPS modules

Dimensions: 269 mm * 267mm * 435mm

6.3. Standard LVPS rack

Designated for up to 8 LVPS modules

| Dimensions: | 483 mm | * 267 m | nm * 435 | mm, 19 | inches rack |
|-------------|--------|---------|----------|--------|-------------|
|-------------|--------|---------|----------|--------|-------------|

| clamp num | signal | color | description |
|-----------|----------|--------|-------------------------------|
| 1 | A1AP+ | orange | Power output (+) chanel A1A |
| 2 | A1AS+ | gray | Sense input (+) chanel A1A |
| 3 | A1AS- | gray | Sense input (-) chanel A1A |
| 4 | A1AP- | blue | Power output (-) chanel A1A |
| 5 | D1AP+ | orange | Power output (+) chanel D1A |
| 6 | D1AS+ | gray | Sense input (+) chanel D1A |
| 7 | D1AS- | gray | Sense input (-) chanel D1A |
| 8 | D1AP- | blue | Power output (-) chanel D1A |
| 9 | D2AP+ | orange | Power output (+) chanel D2A |
| 10 | D2AS+ | gray | Sense input (+) chanel D2A |
| 11 | D2AS- | gray | Sense input (-) chanel D2A |
| 12 | D2AP- | blue | Power output (-) chanel D2A |
| 13 | D3AP+ | orange | Power output (+) chanel D3A |
| 14 | D3AS+ | gray | Sense input (+) chanel D3A |
| 15 | D3AS- | gray | Sense input (-) chanel D3A |
| 16 | D3AP- | blue | Power output (-) chanel D3A |
| 17 | GND | green | Microprocessor and ADC ground |
| 18 | A1BP+ | orange | Power output (+) chanel A1B |
| 19 | A1BS+ | gray | Sense input (+) chanel A1B |
| 20 | A1BS- | gray | Sense input (-) chanel A1B |
| 21 | A1BP- | blue | Power output (-) chanel A1B |
| 22 | D1BP+ | orange | Power output (+) chanel D1B |
| 23 | D1BS+ | gray | Sense input (+) chanel D1B |
| 24 | D1BS- | gray | Sense input (-) chanel D1B |
| 25 | D1BP- | blue | Power output (-) chanel D1B |
| 26 | D2BP+ | orange | Power output (+) chanel D2B |
| 27 | D2BS+ | gray | Sense input (+) chanel D2B |
| 28 | D2BS- | gray | Sense input (-) chanel D2B |
| 29 | D2BP- | blue | Power output (-) chanel D2B |
| 30 | D3BP+ | orange | Power output (+) chanel D3B |
| 31 | D3BS+ | gray | Sense input (+) chanel D3B |
| 32 | D3BS- | gray | Sense input (-) chanel D3B |
| 33 | D3BP- | blue | Power output (-) chanel D3B |
| 34 | TDO+ | gray | JTAG TDO+ (RS485 GI) |
| 35 | TDO- | gray | JTAG TDO- (RS485 GI) |
| 36 | TMS+ | gray | JTAG TMS+ (RS485 GI) |
| 37 | TMS- | gray | JTAG TMS- (RS485 GI) |
| 38 | TCK+ | gray | JTAG TCK+ (RS485 GI) |
| 39 | TCK- | gray | JTAG TCK- (RS485 GI) |
| 40 | TDI+ | gray | JTAG TDI+ (RS485 GI) |
| 41 | TDI- | gray | JTAG TDI- (RS485 GI) |
| 42 | reserved | gray | reserved |

7. Rack Rear Panel Clamps Description

8. Schemes and PCB layout



8.1. LVPS Scheme, Sheet1





8.3. LVPS Scheme, Sheet3



8.4. LVPS Scheme, Sheet4



8.5. LVPS PCB Layout, Component Side



8.6. LVPS PCB Layout, Solder Side